Second Quarterly Progress Report

August 1 through October 31, 1989

NIH project N01-DC-9-2401

"Speech Processors for Auditory Prostheses"

Prepared by

Blake S. Wilson, Charles C. Finley and Dewey T. Lawson

Neuroscience Program Office
Research Triangle Institute
Research Triangle Park, NC 27709

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CONTENTS

I. Introduction

The purpose of this project is to design and evaluate speech processors for implantable auditory prostheses. Ideally, the processors will extract (or preserve) from speech those parameters that are essential for intelligibility and then appropriately encode these parameters for electrical stimulation of the auditory nerve or central auditory structures. Work in the present quarter included the following:

1. Initiation of studies with a recipient (patient JP) of the House Ear Institute (HEI) "Auditory Brainstem Implant" (active electrodes placed on the surface of the ventral cochlear nucleus), in collaboration with R.V. Shannon and J. Wygonski of the HEI (studies were conducted September 18-23 and October 23-27).
2. Follow-up studies with Nucleus patient SW, to begin speech perception studies with her (August 14-18).
3. Follow-up studies with Symbion patient MP, to evaluate additional variations of the "supersampler" processor mentioned in Quarterly Progress Report 1 for this project (October 9-14).
4. Completion of a TMS320C25-based bench processor, for highly-flexible, real-time implementation of "supersampler" and other designs.
5. Further development and application of models of the ensemble of neural responses to intracochlear electrical stimulation (see Quarterly Progress Report 8, NIH project N01-NS-3-2356).
6. Presentation of project results in an invited lecture at the University of Iowa (August 28) and at the 20th Annual Neural Prosthesis Workshop (October 18-20).
7. Preparation for, and conduct of, a project site visit at Duke for Drs. Hambrecht and Heetderks (October 12).
8. Continued preparation of manuscripts for publication.

In this report we present results from the follow-up studies with Symbion patient MP (point 3 above). In addition, we describe the computer interface we have developed for testing patients implanted with the Nucleus device. Results from the studies indicated in points 1, 2, 3 and 5 above will be presented in future reports.

II. New Levels of Speech Perception with Cochlear Implants

The development and application of cochlear prostheses have improved the lives of many deaf individuals. Nearly all patients enjoy remarkable gains in face-to-face communication when the implant is used as an adjunct to lipreading, and some patients can recognize words and sentences with hearing alone. However, the ultimate goal of implant research, full restoration of speech perception without visual cues, has remained elusive. In this report we describe a combination of prosthesis elements that produces a close approximation to normal perception for an implant patient.

A cochlear prosthesis consists of (a) a microphone to sense the acoustic environment, (b) a speech processor to transform the microphone signal into stimuli for direct activation of the auditory nerve, (c) a transcutaneous or percutaneous transmission system for sending stimulus information to implanted electrodes, and (d) the electrodes. The electrodes for a multichannel implant usually are inserted as an array into the scala tympani. This places the electrodes close to residual auditory neurons. In cases of good nerve survival, use of different electrodes can produce shifts in the populations of excited neurons (*1,2*).

Processors

The purpose of the present study was to compare strategies for the speech processor in tests with an implant patient who had excellent performance with his standard, clinical device. The strategies included the *compressed analog* (CA) processor used in the clinical device, and the alternative *interleaved pulses* (IP) and *supersampler* (SS) processors. All strategies made use of the tonotopic organization of the auditory nerve by stimulating electrodes near the apex of the cochlea to indicate the presence of low-frequency sounds and by stimulating electrodes near the base of the cochlea to indicate the presence of high-frequency sounds. However, other details of the stimulation patterns were quite different among strategies.

Waveforms of the three processing strategies are shown in Fig. 1. The CA processor first compresses the wide dynamic range of input speech signals into the narrow dynamic range available for electrical stimulation of the auditory nerve. The compressed signal then is filtered into frequency bands for presentation to each electrode. Filtered output signals for four channels of intracochlear stimulation are illustrated in the figure. The inputs include segments of voiced (/ɔ/) and unvoiced (/t/) speech. During the voiced segment the relatively large outputs of apical channels 1 and 2 reflect the low-frequency formant content (spectral peaks) of the vowel, and the clear periodicity in these waveforms reflects the fundamental and first formant frequencies. During unvoiced speech the stimuli are aperiodic and have greater amplitudes in the higher (more basal) channels.

A concern associated with the use of CA processors is that of channel interactions (*3*). Simultaneous stimulation of two or more channels with continuous waveforms results in summation of the electrical fields from the different electrodes. This summation can exacerbate interactions among channels, especially for patients who require high stimulation levels.

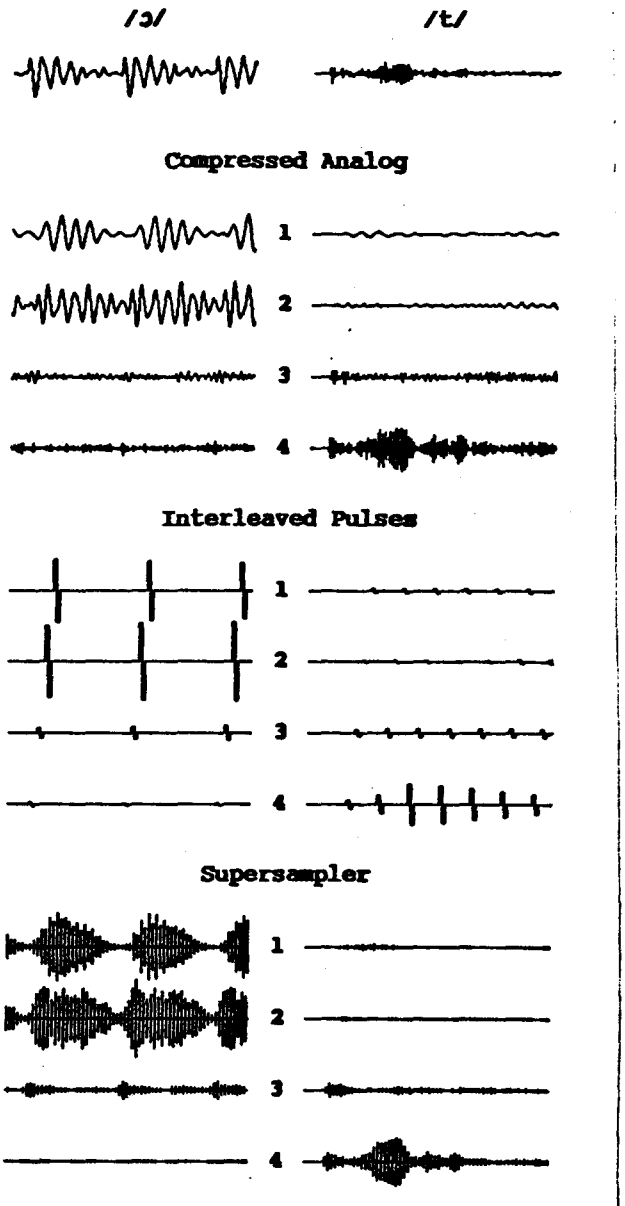


Fig. 1. Waveforms of three processing strategies. Equalized (6 dB/octave attenuation below 1200 Hz) speech inputs are shown at the top and stimulus waveforms for each of the strategies at the bottom. The left column shows an input and stimulus waveforms for a voiced speech sound and the right column those traces for an unvoiced speech sound. Stimulus waveforms are numbered by channel, with channel 1 delivering its output to the apical-most electrode in the scala tympani. Center frequencies for the bandpass filters associated with channels 1-4 are 0.5, 1.0, 2.0, and 4.0 kHz respectively. The time constants of the integrating filters for bandpass energy detection are 8.0 ms in the IP strategy and 0.4 ms in the SS strategy. The duration of each trace is 25.4 ms.

The problem of channel interactions is addressed in the IP and SS processors through the use of nonsimultaneous stimuli. There is no temporal overlap between stimulus pulses, so that direct summation of electrical fields is avoided. The energy in each frequency band of the input signal is represented by the amplitudes of the pulses delivered to each electrode. The pulses shown in Fig. 1 have a one-to-one correspondence with the root-mean-square (RMS) energies in each band. In actual applications of the IP and SS processors, pulse amplitudes are determined with a logarithmic transformation (*4*) of RMS energies to compress the dynamic range of those energies into the range of electrically-evoked hearing.

Differences between the IP and SS processors are ones of rates of stimulation and of the way in which voiced and unvoiced segments are treated. In the IP processor distinctions between voiced and unvoiced segments are represented by the timing of cycles of stimulation across the electrode array. During voiced segments stimulation cycles are presented at the fundamental frequency of the speech sound, and during unvoiced segments stimulation cycles are presented either at a fixed, high rate or at randomly-varied intervals.

In contrast, the SS processor presents stimulation cycles at the maximum rate (with one cycle immediately following its predecessor) during both voiced and unvoiced segments. In addition, the SS processor generally uses the shortest possible durations for pulses and intervals between pulses so that rapid variations in RMS energies can be followed ("sampled") by variations in pulse amplitudes for each channel.

Methods

The processors of Fig. 1 were evaluated with a variety of speech perception tests. Because the subject had excellent performance with his CA processor, only the most difficult tests normally administered to implant patients were used. These included identification of 16 consonants (/b, d, f, g, dʒ, k, l, m, n, p, s, ʃ, t, ð, v, z/) in an /a/-consonant-/a/ context (*5*) and the open-set tests of the Minimal Auditory Capabilities battery (*6*). In the consonant test multiple exemplars of the /aCa/ tokens were played from laser videodisc recordings of a male speaker and a female speaker. A single block of trials consisted of five randomized presentations of each consonant for one of the speakers. Ten blocks were administered for the CA processor and four blocks each for the IP and SS processors (*7,8*).

The open-set tests included recognition of 50 one-syllable words from Northwestern University Auditory Test 6 (NU-6); 25 two-syllable words (spondees); 100 key words in the Central Institute for the Deaf (CID) sentences of everyday speech; and the final word in 50 high-context (WIC) sentences. In these tests single presentations of the words or sentences were played from cassette tape recordings of a male speaker.

In addition to the above, two tests were administered for further evaluation of the CA and SS processors. These were the recognition of key words in the low-context IEEE/Harvard sentences (*9*) and connected discourse tracking (*10,11*). In the IEEE/Harvard test blocks of 10 sentences were played from the audio track of videotape recordings. Each block contained 50 key words, with the utterances made by a male or female speaker. Four blocks were administered for

the CA processor and two blocks for the SS processor (*7*). New sets of sentences, balanced for difficulty, were used for each block.

All tests were conducted with hearing alone, and all tests except tracking used single presentations of recorded material with no feedback on correct or incorrect responses. In the tracking test the subject's task was to repeat verbatim previously-unknown paragraphs read by a trained speaker (*11*). For items not understood after the first presentation, various strategies such as repetition of phrases or words were used until the items were correctly repeated. The test score was calculated by dividing the time taken to complete four paragraphs by the number of words in those paragraphs. Scores for the remaining tests were calculated as the percentage of correct responses. In addition, results for the consonant identification test were expressed as percent information transfer for articulatory and acoustic features that characterize the selected consonants (*12,13*).

As mentioned before, the subject's own clinical device (the Symbion prosthesis) was used for the tests with the CA processor. The implementations of the IP and SS processors were selected by evaluating several variations of each with the consonant identification test. The variations with the best scores then were used for the full battery of remaining tests. Six channels of stimulation were used for the IP and SS processors (*14,15*) and four channels for the CA processor (*16*). Detailed information on the clinical CA processor may be found in papers by Eddington (*17*), and additional parameters of the IP and SS processors are presented in Table 1.

Table 1. Parameters of the interleaved pulses (IP) and supersampler (SS) processors. The pulse parameters include duration per phase (dur/ph) and separation between pulses (sep), and the remaining parameters include the time constant of the integrating filters for bandpass energy detection (RMS integrator), the frequency below which speech signals are attenuated for input equalization (eq), the sequence of channels for each stimulation cycle (channel sequence; channel 6 is the most basal), and the rate of pulsatile stimulation on each channel (rate). The rate for the IP processor is that used during unvoiced segments.

	Pulses (μs)					
Proc	dur/ph	sep	RMS integrator (ms)	eq (Hz)	Channel sequence	rate (Hz)
IP	100	0	8.0	1200	6-5-4-3-2-1	278
SS	55	0	0.2	600	6-3-5-2-4-1	1515

Results

Results for the consonant identification test are presented in Fig. 2. The percent correct and feature transmission scores demonstrate a clear picture of relative performance among processors. That is, despite four years of daily experience with the CA processor, the IP and SS processors immediately produce superior scores. Use of the IP strategy produces gains over the CA strategy for every feature except voicing (where scores are about the same), and use of the SS strategy produces gains over both the IP and CA processors for all features. Especially large increases shared by the IP and SS processors include those for nasality and place of articulation. In addition, substantial increases in the scores for voicing, frication, and duration are obtained when the SS strategy is used instead of the IP strategy.

Because scores for the SS processor approximate the ceilings of perfect performance, the increases shown in Fig. 2 may in fact underestimate the relative superiority of that processor. In particular, the scores for overall percent correct, overall information transfer, voicing, nasality, duration, and envelope are 92% or higher.

The ranking of processors suggested by the consonant results is affirmed in the results of the remaining tests, presented in Fig. 3. For the tests with results not at the ceiling of either extremely-high (spondee recognition) or perfect (CID sentences) scores, the IP processor produces scores that are equivalent or superior to those of the CA processor, and the SS processor produces scores that are clearly superior to those of both.

Discussion

To our knowledge, the scores obtained with the SS processor exceed all published results for cochlear implants by wide margins. Also, these scores demonstrate a close approximation to normal speech perception with a cochlear implant.

The performance of the SS processor may be explained in terms of its design. The high rate of stimulation on each channel probably allowed the subject to perceive details in the temporal variations of band energies, while the use of nonsimultaneous stimuli eliminated a principal component of channel interactions. Indeed, results from the consonant test are fully consistent with these ideas. Feature transmission scores for nasality and place of articulation, which are largely represented by channel cues (*12,13*), are improved with the use of either the IP or SS processors. Scores for the remaining consonant features, which are largely or solely represented by temporal variations (*12,18*), are improved with the SS processor.

Finally, the electrode array and the subject probably played major roles in the outcome of the present tests. Results from psychophysical studies with this subject indicated that he (a) could rank his electrodes in an appropriate tonotopic order according to pitch percepts produced by stimulation of each electrode, (b) had low levels of measured channel interactions for nonsimultaneous stimuli, and (c) had extremely low thresholds for a variety of stimuli. These results are consistent with a picture of excellent nerve survival (*2,19*). Such survival, in conjunction with the multichannel electrode array, may have been essential to the perception of the temporal and

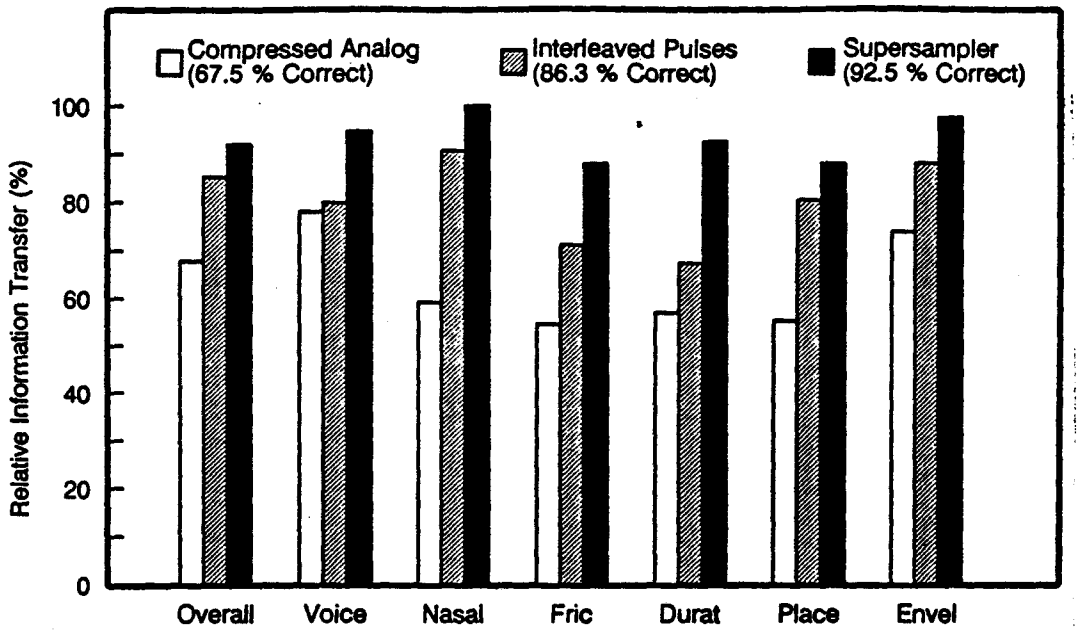


Fig. 2. Relative information transfer for consonant features. The features include voicing (voice), nasality (nasal), place of articulation (place), duration (durat), frication (fric), and envelope cues (envel).

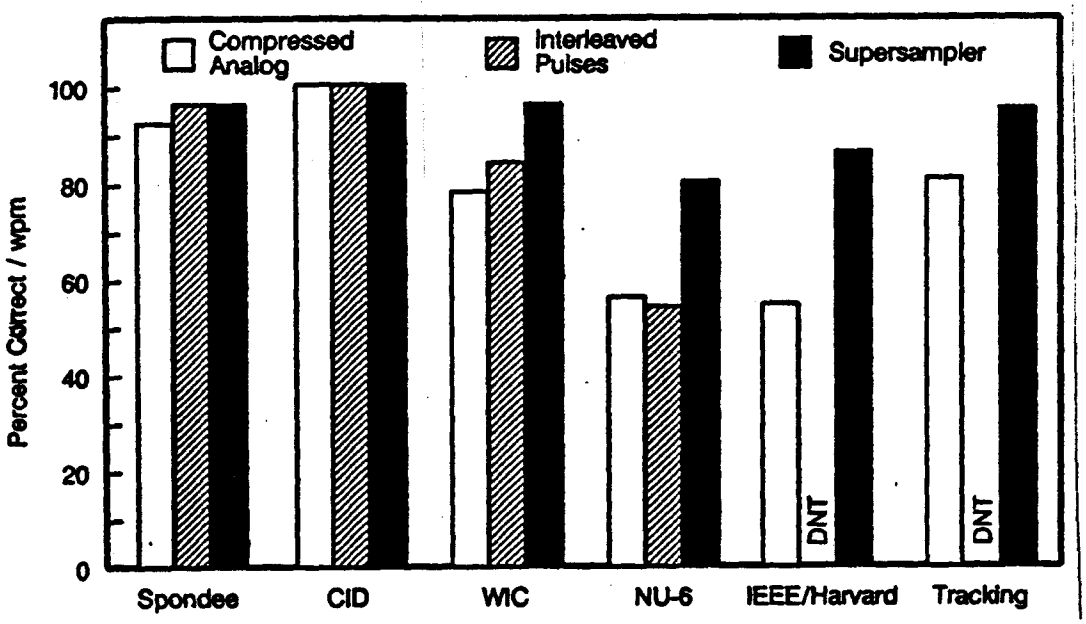


Fig. 3. Scores from the open-set tests. The scores for the tracking test are given in words per minute, and the scores for the remaining tests are given as percent correct.

spatial representations provided by the SS processor.

In conclusion, results of this study demonstrate a combination of prosthesis elements that can bring a person from total deafness (*20*) to nearly normal perception of speech with hearing alone. Our present challenge is produce similar results across a population of patients with varying degrees of nerve survival.

Acknowledgements

We are pleased to acknowledge the collaboration of R.D. Wolford, D.K. Eddington and W.M. Rabinowitz is the studies with MP. We also are indebted to MP for his precise descriptions of speech percepts and for his enthusiastic participation.

References and Notes

1. R. Hartmann and R. Klinke, in *Cochlear Implants: Models of the Electrically Stimulated Ear*, J.M. Miller and F.A. Spelman, Eds. (Springer-Verlag, New York, 1990), pp. 135-159; C. van den Honert and P.H. Stypulkowski, *Hearing Res.* **29**, 195 (1987).
2. M.M. Merzenich and M.W. White, in *Functional Electrical Stimulation*, F.T. Hambrecht and J.B. Reswick, Eds. (Dekker, New York, 1977), pp. 321-340.
3. M.W. White, M.M. Merzenich and J.N. Gardi, *Arch. Otolaryngol.* **110**, 493 (1984); B.S. Wilson, C.C. Finley, D.T. Lawson and R.D. Wolford, *Proc. IEEE* **76**, 1143 (1988).
4. B.S. Wilson *et al.*, *Laryngoscope* **98**, 1069 (1988).
5. R.S. Tyler, J.P. Preece and M.W. Lowder, *The Iowa Audiovisual Speech Perception Laser Videodisc*, Laser videodisc and laboratory report (University of Iowa, Department of Otolaryngology, Iowa City, IA, 1987); D.T. Lawson, B.S. Wilson and C.C. Finley, *Fourteenth Quarterly Progress Report*, NIH contract N01-NS-5-2396 (Neural Prosthesis Program, Bethesda, MD, 1989).
6. E. Owens, D.K. Kessler, M. Raggio and E.D. Schubert, *Ear Hear.* **6**, 280 (1985).
7. An equal number of blocks was used for the male and female speakers.
8. The blocks for the CA processor were spread throughout the testing period to evaluate the possibility of learning effects. Results from those blocks were highly repeatable and thus no evidence of such effects was obtained.
9. W.M. Rabinowitz, K.W. Grant and D.K. Eddington, *J. Acoust. Soc. Am.* **84**, S45 (1988).
10. C.L. De Filippo and B.L. Scott, *J. Acoust. Soc. Am.* **63**, 1186 (1978).
11. E. Owens and M. Raggio, *J. Speech Hear. Disorders* **52**, 120 (1987).
12. G.A. Miller and P.E. Nicely, *J. Acoust. Soc. Am.* **27**, 338 (1955).
13. B.S. Wilson, C.C. Finley and D.T. Lawson, in *Cochlear Implants: Models of the Electrically Stimulated Ear*, J.M. Miller and F.A. Spelman, Eds. (Springer-Verlag, New York, 1990), pp. 339-376.

14. Results from previous studies with the present subject demonstrated a slight superiority of a 6-channel IP processor over a 4-channel variation of the same processor (see *QPR 1*, this project).
15. Bandpasses for both processors were spaced along a logarithmic scale to span frequencies between 350 and 7000 Hz.
16. The outputs of the IP and SS processors were delivered via isolated current sources to the six monopolar electrodes of the Symbion implant, and the outputs of the CA processor were delivered to the apical four of those electrodes.
17. D.K. Eddington, *J. Acoust. Soc. Am.* **68**, 885 (1980); D.K. Eddington, *Ann. N.Y. Acad. Sci.* **405**, 241 (1983).
18. D.J. Van Tassell, S.D. Soli, V.M. Kirby and G.P. Widin, *J. Acoust. Soc. Am.* **82**, 1152 (1987).
19. J.N. Gardi, in *Cochlear Implants*, R.A. Schindler and M.M. Merzenich, Eds. (Raven Press, New York, 1985), pp. 351-363; M.M. Merzenich, P. Leake-Jones, M. Vivion, M. White and M. Silverman, *Fourth Quarterly Progress Report*, NIH contract N01-NS-7-2367 (Neural Prosthesis Program, Bethesda, MD, 1978); B.E. Pfingst, I. Glass, F.A. Spelman and D. Sutton, in *Cochlear Implants*, R.A. Schindler and M.M. Merzenich, Eds. (Raven Press, New York, 1985), pp. 305-322; B.E. Pfingst and D. Sutton, *Ann. N.Y. Acad. Sci.* **405**, 224 (1983); R.V. Shannon, *Hearing Res.* **12**, 1 (1983).
20. Prior to the implant, the subject's hearing levels at octave intervals from 125 Hz to 4000 Hz were 93, 113, 126, 131, 134, and 128 dB respectively.

III. Plans for the Next Quarter

Our plans for the next quarter include the following:

1. Follow-up studies with UCSF/Storz patient MC2 (December 11-16).
2. Studies with additional Symbion patients (one patient, SS, is tentatively scheduled for November 27 to December 2).
3. Begin design and construction of portable speech processors, for evaluation of learning effects with Symbion subjects RB and MP. These processors will be capable of implementing the "interleaved pulses" and "supersampler" strategies, and will be based on the TMS320C25 device. Studies to evaluate learning effects with those strategies will be conducted in collaboration with Drs. Eddington and Rabinowitz of the Massachusetts Eye and Ear Infirmary and the Massachusetts Institute of Technology.
4. Preparation of invited papers to be published in (a) the special issue of Am. J. Otol. on "Cochlear Implants in Young Children" and (b) the book *Behavioral Aspects of Speech Technology: Theory and Applications*, edited by A.K. Syrdal, R. Bennett and S. Greenspan.
5. Presentation of project results in invited lectures at (a) the *Eleventh Annual Conference on Engineering in Medicine and Biology*, to be held in Seattle (Finley, November 8-12); (b) the House Ear Institute in Los Angeles (Finley, November 15); and (c) the *Third Symposium on Cochlear Implants in Children: Current Status and Future Directions*, to be held in Indianapolis (Wilson, January 26-27).

Appendix 1

Summary of Reporting Activity for the Period of
August 1 through October 31, 1989

NIH Contract N01-DC-9-2401

Wilson, B.S.: Comparison of analog and pulsatile coding strategies for multichannel cochlear prostheses. Invited speaker presentation, Department of Otolaryngology -- Head & Neck Surgery, University of Iowa at Iowa City, August 28, 1989.

Wilson, B.S.: Speech processors for auditory prostheses. Presented at the *20th Annual Neural Prosthesis Workshop*, National Institutes of Health, Bethesda, MD, October 18-20, 1989.

Appendix 2

Computer Interface for Testing Patients Implanted with the Nucleus Device

Prepared by

Dewey T. Lawson

A highly flexible computer interface has been developed for testing patients implanted with the Nucleus 22-electrode cochlear prosthesis. The interface is composed of two pieces of software--one running on the central processor of a standard personal computer (PC) and the other on a TMS320C25 coprocessor, part of a Spectrum (Loughborough Sound Images) Development Board installed within the PC.

AWAKE, the program executing on the coprocessor, controls the XF pin of the TMS320C25, providing the DAMP signal identified in Figure 21, U. S. Patent 4,532,930 for the Nucleus prosthesis. The same XF line also is used to gate the coprocessor's CLOCKOUT2 signal in order to form the OUTPUT signal indicated in the same patent figure. Virtually no hardware is needed for the interface, beyond the PC and its coprocessor board. AWAKE relays to the Nucleus implant system control sequences supplied to it by the PC. Whenever 50 msec passes without a sequence being ordered to control patient stimulation, AWAKE transmits a valid but non-stimulating sequence to maintain operation of the implanted receiver.

Any patient testing program running on the PC can construct one or more valid control sequences anywhere in memory and then cause their transmission to the implanted system with a single call to the subroutine NUCCYC. The arguments passed to NUCCYC are the initial segment and offset addresses in the PC's memory, the number of words to be sent, and the number of times to send them. Each valid control sequence is six 16-bit words long.

To document the interface design and make it available, the remainder of this appendix is comprised of the following documents:

1. An outline of the six-word control sequence format for use in writing main programs to run on a PC.

2. An outline of the handshaking arrangements governing interactions between the PC and the coprocessor board once AWAKE is running.

3. A listing of NUCCYC in a C Language form that can be compiled by Borland's Turbo C version 2.0

4. Listings of NUCSTART and NUCSTOP, C Language subroutines that, respectively, start and stop AWAKE once it has been loaded into the Development Board's memory. These routines can be compiled by Turbo C as well.

5. A listing of AWAKE in a form that can be assembled with the Texas Instruments 320C25 Family Macro Assembler version PC 3.0 87.055.

A version of NUCCYC callable from programs compiled by Lahey Computer Systems FORTRAN-77 3.01 also has been written in C Language. The only changes necessary were (1) to define the subroutine type as "void" so that it returns no function value, eliminating the error return, and (2) to pass argument pointers [int *seg, int *offset, int *nvords, and int *ncycles] and then alias the arguments to internal variables for use in the subroutine's inline asm statements.

Outline of the six-word control sequence format for commands to the Nucleus 22-Electrode interface:

["fix( )" signifies rounding off the argument to the nearest integer]

1st word

more significant byte = 8n + 3
where n is id number of electrode [1..22]

less significant byte = 11 for common ground mode
or, for bipolar mode with electrode number m:

```
8(m - n) + 11        if m >  n
8(22 + m - n) + 11   if m <= n
```

[m = n can be useful for constructing control sequences that produce no output pulse]

2nd word

16 + fix(log(a) / log(0.97))
where a is, approximately, current in milliamperes
[for precise current specification, the calibration curve must be obtained for the individual device]

3rd word

fix(p / 0.4)
where p is pulse duration per phase in microseconds

4th word

fix(s / 0.4)
where s is interphase separation in microseconds

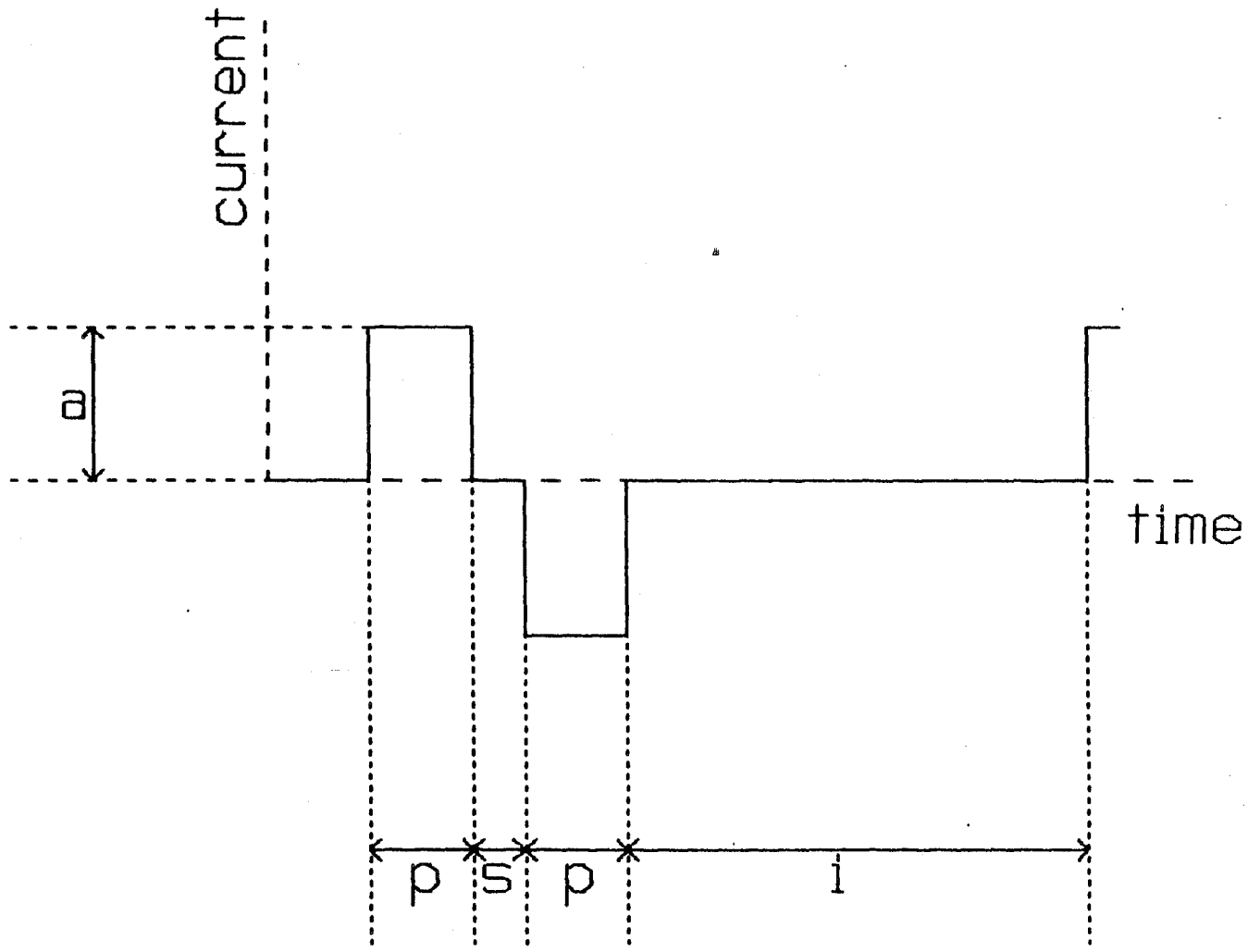
5th word

least significant 16 bits of fix(i / 0.4)
where i is interpulse interval in microseconds

6th word

less significant byte = repeat count for 5th word
[most significant byte in three-byte number fix(i / 0.4)]

more significant byte not used


current
a
time
p
s
p
i

Outline of the handshaking between the host PC and the TMS320C25 on the Spectrum Board:

PC	TMS320C25
lovers control byte bit 4	
	finds status bit 4 lov
	writes to port 0, raising status bit 1
finds status bit 1 high, lovering status bit 1 [and bit 0]	
writes to port	
raises control byte bit 4	
	finds status bit 4 high
	reads port, raising status bit 0
finds status bit 0 high lovering status bit 0 [and bit 1]	

```
/*
   NUCCYC.C

   a C Language subroutine for sending six-word control sequences from a PC
   to the program AWAKE running on a Spectrum (Loughborough Sound Images)
   TMS320C25 Development Board

   arguments passed to the subroutine include the segment and offset in PC
   memory at which the control sequence begins, the number of words in the
   sequence, and the number of cycles of that sequence to be sent

   normal return is with a function value of zero, while a 1 on return
   signals that the TMS320C25 coprocessor is not running

   REFERENCE POINTS A-D correspond to those in the AWAKE listing

   version of 22 March 1989

*/


int nuccyc(unsigned int seg, unsigned int offset, unsigned int nwords, unsigned int ncycles)
 {
  const int port = 0x290;
  const unsigned char c4l = 0xc0;
  const unsigned char c4h = 0xd0;
  asm push es;
  asm push ds;
  asm push dx;
  asm push cx;
  asm push bx;
  asm push ax;
  asm mov es,seg;                  /* set data segment                          */
  asm mov dx,port;                 /* preset status port id                     */
  asm add dx,4;
  asm mov ax,ncycles;              /* preset for preserve                       */
 CYCLE:
  asm mov ncycles,ax;              /* preserve cycle count                      */
  asm mov bx,offset;               /* preset data address                       */
  asm mov cx,nwords;               /* preset word count                         */
 NOT_YET:
  asm mov al,c4l;                  /* control byte w bit 4 low                  */
  asm out dx,al;                   /* send control byte      REFERENCE POINT A  */
  asm in al,dx;                    /* read status                               */
  asm test al,64;                  /*  is Coprocessor running?                  */
  asm jz ERROR;                    /*  if not, get out                          */
  asm test al,2;                   /*  if so check status bit 1                 */
  asm jz NOT_YET;                  /*  back if not ready                        */
                                   /*  (status bit 1 high)   REFERENCE POINT B  */
  asm mov ax,word ptr es:[bx];     /* pointer to next word                      */
  asm mov dx,port;                 /* set to data port                          */
  asm out dx,ax;                   /* send word                                 */
  asm add dx,4;                    /* set to status port                        */
  asm mov al,c4h;                  /* control byte w bit 4 high                 */
  asm out dx,al;                   /* send control byte      REFERENCE POINT C  */
  asm inc bx;                      /* point to next word                        */
```

```
 asm inc bx;
CHECK:
 asm in al,dx;                  /* check status bit 0                      */
 asm test al,1;                 /*   has Coprocessor read?                 */
 asm jz CHECK;                  /*   if not, wait for it                   */
                                /*   (status bit 0 high)   REFERENCE POINT D */
 asm dec cx;                    /* decrement word count                    */
 asm jnz NOT_YET;               /*     continue if not 0                   */
 asm mov ax,ncycles;            /* get cycle count                         */
 asm dec ax;                    /*     and decrement it                    */
 asm jnz CYCLE;                 /*     continue if not 0                   */
OUTNOW:                         /*     normal return if 0                  */
 asm pop ax;
 asm pop bx;
 asm pop cx;
 asm pop dx;
 asm pop ds;
 asm pop es;
 return 0;
ERROR:
 asm pop ax;
 asm pop bx;
 asm pop cx;
 asm pop dx;
 asm pop ds;
 asm pop es;
 return (1);
}
```

```
/*  NUCSTART.C

    a C Language subroutine that will reset and then start the
    program AWAKE previously loaded to a Spectrum (Loughborough
    Sound Images) TMS320C25 Development Board

    version of 23 March 1989

*/

void nucstart(void)
{
  const int port = 0x290;
  const unsigned char cal = 0x00;
  const unsigned char c7h = 0xd0;
  asm push es;
  asm push ds;
  asm push dx;
  asm push cx;
  asm push bx;
  asm push ax;
  asm mov dx,port;
  asm add dx,4;
  asm mov al,cal;
  asm out dx,al;
  asm mov al,c7h;
  asm out dx,al;
  asm pop ax;
  asm pop bx;
  asm pop cx;
  asm pop dx;
  asm pop ds;
  asm pop es;
}
```

```
/*  NUCSTOP.C

    a C Language subroutine that will assert the hold line of a
    Spectrum (Loughborough Sound Images) TMS320C25 Development Board,
    stopping execution of the AWAKE program

    version of 23 March 1989

*/

void nucstop(void)
{
  const int port = 0x290;
  const unsigned char c7h = 0xc0;
  asm push es;
  asm push ds;
  asm push dx;
  asm push cx;
  asm push bx;
  asm push ax;
  asm mov dx,port;
  asm add dx,4;
  asm mov al,c7h;
  asm out dx,al;
  asm pop ax;
  asm pop bx;
  asm pop cx;
  asm pop dx;
  asm pop ds;
  asm pop es;
}
```

```
      IDT 'AWAKE'
*
*     AWAKE.ASM interface driver
*
*
*     Assembler code for a program that executes on a Spectrum
*     (Loughborough Sound Images) TMS320C25 Development Board
*     and outputs control sequences for a standard Nucleus
*     cochlear prosthesis processor output stage via the XF and
*     CLOCKOUT2 pins of the TMS320C25.
*
*     (XF supplies the DAMP signal, and is used to gate CLOCKOUT2 to
*     form the OUTPUT signal, of Figure 21, U.S. Patent 4,532,930)
*
*     A background task is included, to transmit a valid but non-
*     stimulating code sequence every 50 msec to maintain operation
*     of the patient's implanted receiver in the absence of any
*     meaningful sequence ordered by the host PC.
*
*      REFERENCE POINTS A-D in the comments correspond to those in the
*      NUCCYC listing
*
*      version of 22 March 1989
*
* Address constants
*

BLK1   EQU    8       ;Page 8 of Data Mem is start of Extern Mem
ELEMOD EQU    0
MODE   EQU    1
ELECT  EQU    2
AMPL   EQU    3
PHASE  EQU    4
INTRPH EQU    5
DLYCNT EQU    6
DLYRPT EQU    7
TEMP   EQU    8
VPOS   EQU    9
VNEG   EQU    )A
VZERO  EQU    )B
DLNRPT EQU    )C
DLYLEN EQU    )D

*
* Parameter constants
*

SYNC   EQU    3
DAC    EQU    3
PRT0   EQU    0
PRT1   EQU    1

*
* Parameters for background (maintenance) control sequence
*
```

```
DMYCNT EQU     2500    ;0.4 usec ticks per 1.0 msec delay
DMYRPT EQU     50      ;1.0 msec delays per 50 msec maintenance interval
DELECT EQU     139     ;17th chosen as active electrode
DMODE  EQU     187     ;offset of 23 chooses SAME electrode as reference
DAMP   EQU     272     ;maximum duration for minimum stimulus amplitude
DPHASE EQU     11      ;11 ticks--4.4 usec--per phase
DINTRP EQU     47      ;allow same interphase interval as Nucleus clinical system
DMYLEN EQU     47      ;allow same interburst interval as Nucleus clinical system

*
*  Program
*

       AORG    )0
       B       BEGIN   ;branch to code on reset
       AORG    )500
BEGIN  CNFP
       LARP    1
       LDPK    BLK1
*                       initialize sequence parameters to safe values
       LACK    DELECT
       SACL    ELECT
       LACK    DMODE
       SACL    MODE
       LALK    DAMP
       SACL    AMPL
       LAC     DPHASE
       SACL    PHASE
       LAC     DINTRP
       SACL    INTRPH
       LALK    DMYCNT
       SACL    DLYCNT
       LAC     DMYRPT
       SACL    DLYRPT
       LACK    0
       SACL    TEMP
       LRLK    AR1,DMYCNT      ;setup counter for ticks per unit
       LRLK    AR2,DMYRPT      ;setup counter for delays per maintenance interval

*
*  Input of six-word parameter set from host PC
*

LOOP   NOP

A1     BIOZ    B1      ;watch for control bit 4 being cleared by PC
*                                                       REFERENCE POINT A
       BANZ    A1,*-   ;meanwhile, keep track of maintenance interval
       CALL    DUMMY   ;and send maintenance sequence every 50 ms
       B       A1

B1     OUT     TEMP,PRT0                               ;REFERENCE POINT B
*                       write to port 0, setting status bit 1 high
C1     BIOZ    C1      ;wait until control bit 4 is set high by PC
*                                                       REFERENCE POINT C
       IN      ELEMOD,PRT0                             ;REFERENCE POINT D
```

```
*                    read port 0, store data, setting status bit 0 high

        LAC     ELEMOD,0        ;extract MODE
        ANDK    )FF
        SACL    MODE,0

        LAC     ELEMOD,0        ;extract ELECT
        RPTK    7
        SFR
        ANDK    )FF
        SACL    ELECT,0

A2      BIOZ    B2      ;wait until control bit 4 is cleared by PC
*                                                       REFERENCE POINT A
        B       A2
B2      OUT     TEMP,PRT0                               ;REFERENCE POINT B
*                write to port 0, setting status bit 1 high
C2      BIOZ    C2      ;wait until control bit 4 is set high by PC
*                                                       REFERENCE POINT C
        IN      AMPL,PRT0                               ;REFERENCE POINT D
*                read port 0, store data, setting status bit 0 high

A3      BIOZ    B3                      ;et c.
        B       A3
B3      OUT     TEMP,PRT0
C3      BIOZ    C3
        IN      PHASE,PRT0

A4      BIOZ    B4
        B       A4
B4      OUT     TEMP,PRT0
C4      BIOZ    C4
        IN      INTRPH,PRT0

A5      BIOZ    B5
        B       A5
B5      OUT     TEMP,PRT0
C5      BIOZ    C5
        IN      DLYCNT,PRT0

A6      BIOZ    B6
        B       A6
B6      OUT     TEMP,PRT0
C6      BIOZ    C6
        IN      DLNRPT,PRT0

        LAC     DLNRPT,0        ;extract DLYRPT
        ANDK    )FF
        SACL    DLYRPT,0

        LAC     DLNRPT,0        ;extract DLYLEN
        RPTK    7
        SFR
        ANDK    )FF
        SACL    DLYLEN,0
```

```
SKIP   CALL    DOIT    ;transmit the sequence just ordered by the host PC
       B       LOOP    ;then back to maintenance/receive mode

*
*  Subroutine DOIT for output of a sequence ordered by host PC
*

*    sync burst

DOIT   LARK    AR1,SYNC
       LARP    1
L1     RXF             ;XF is reset during bursts
       BANZ    L1,*-

*    interburst interval

       SXF             ;XF is set immediately at end of each burst
       LAR     AR1,DLYLEN
D1     SXF             ;XF remains set between bursts
       BANZ    D1,*-

*    active electrode burst

       LAR     AR1,ELECT
L2     RXF             ;et c.
       BANZ    L2,*-

*    interburst interval

       SXF
       LAR     AR1,DLYLEN
D2     SXF
       BANZ    D2,*-

*    electrode mode burst

       LAR     AR1,MODE
L3     RXF
       BANZ    L3,*-

*    interburst interval

       SXF
       LAR     AR1,DLYLEN
D3     SXF
       BANZ    D3,*-

*    amplitude burst

       LAR     AR1,AMPL
L4     RXF
       BANZ    L4,*-

*    interburst interval

       SXF
```

```
        LAR     AR1,DLYLEN
D4      SXF
        BANZ    D4,*-

*   phase 1 burst

        LAR     AR1,PHASE
L5      RXF
        BANZ    L5,*-

*   interphase interval

        SXF
        LAR     AR1,INTRPH
D5      SXF
        BANZ    D5,*-

*   phase 2 burst

        LAR     AR1,PHASE
L6      RXF
        BANZ    L6,*-

*   interpulse interval

        SXF
IPIDLY  LAR     AR2,DLYRPT
IPIDLA  LARP    1
        LAR     AR1,DLYCNT
D6      SXF
        BANZ    D6,*-
        LARP    2
        BANZ    IPIDLA,*-
        LARP    1

*   reset counters to begin a new maintenance interval

        LRLK    AR1,DMYCNT
        LRLK    AR2,DMYRPT

        RET                     ;end of subroutine DOIT

*
*  Subroutine DUMMY for output of a maintenance sequence
*

DUMMY   LARP    2
        BANZ    DOUT,*-
        B       DSTRT
DOUT    LARP    1               ;if still within maintenance interval
        LRLK    AR1,DMYCNT      ;return to await orders from the host PC
        RET

*   sync burst

DSTRT   LARK    AR1,SYNC        ;if maintenance interval has elapsed
```

```
        LARP    1               ;proceed to transmit a maintenance
DL1     RXF                     ;sequence to the patient's implanted receiver
        BANZ    DL1,*-

*   interburst interval

        SXF
        LARK    AR1,DMYLEN
DD1     SXF
        BANZ    DD1,*-

*   active electrode burst

        LARK    AR1,DELECT
DL2     RXF
        BANZ    DL2,*-

*   interburst interval

        SXF
        LARK    AR1,DMYLEN
DD2     SXF
        BANZ    DD2,*-

*   electrode mode burst

        LARK    AR1,DMODE
DL3     RXF
        BANZ    DL3,*-

*   interburst interval

        SXF
        LARK    AR1,DMYLEN
DD3     SXF
        BANZ    DD3,*-

*   amplitude burst

        LRLK    AR1,DAMP
DL4     RXF
        BANZ    DL4,*-

*   interburst interval

        SXF
        LARK    AR1,DMYLEN
DD4     SXF
        BANZ    DD4,*-

*   phase 1 burst

        LARK    AR1,DPHASE
DL5     RXF
        BANZ    DL5,*-
```

```
*    interphase interval

       SXF
       LARK    AR1,DINTRP
DD5    SXF
       BANZ    DD5,*-

*    phase 2 burst

       LARK    AR1,DPHASE
DL6    RXF
       BANZ    DL6,*-

*    interpulse interval

       SXF

*    reset for maintenance interval countdown

       LARP    1
       LRLK    AR1,DMYCNT
       LRLK    AR2,DMYRPT

       RET                     ;end of subroutine DUMMY

       END
```