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Speech Processors for Auditory Prostheses

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I. Introduction

The purpose of this project is to design and evaluate speech processors for implantable auditory prostheses. Ideally, the processors will extract (or preserve) from speech those parameters that are essential for intelligibility and then appropriately encode these parameters for electrical stimulation of the auditory nerve or central auditory structures. Work in the present quarter included the following:

1. Completion of a prototype portable processor, based on the Motorola DSP 56001, for evaluation of the *continuous interleaved sampling* (CIS) strategy in field trials.
2. Development of monitor and other software for the DSP 56001 system.
3. Development of automated testing procedures for functional evaluations of CIS processor implementations.
4. Initial development of isolated interfaces between a controlling PC computer and the DSP 56001 unit, for safe use of the combined system in the laboratory.
5. Initial development of a shell program that will allow high-level specification of parameters for CIS processors, and subsequent incorporation of those parameters, in a compiled program for execution on the DSP 56001 platform.
6. Renewed studies with patient UP3 (formerly referred to as patient MH), primarily to evaluate the CIS strategy with a patient who has the UCSF/Storz electrode array and a percutaneous connector.
7. Continued collaboration with Robert Shannon and others at the House Ear Institute, to evaluate the *continuous sampling* (CS) strategy with additional auditory brainstem implant (ABI) patients.
8. Presentation of project results at *Surgical Grand Rounds*, Duke University Medical Center (Finley).
9. Continued preparation of manuscripts for publication.

In this report we describe work related to points 1, 2 and 4 above. Results from work in the other indicated areas will be presented in future reports.

II. A Wearable Speech Processor Platform for Auditory Research

A. General overview

1. Basic requirements

The objective of this speech processor design is a powerful and highly flexible platform for the implementation of a wide parametric and architectural range of real-time signal processing strategies. A variety of output interface options for different implant systems and transducer devices are accommodated. The system is intended as a research tool for testing advanced speech processor designs over extended periods of wear by patients during normal daily activities.

Such a speech processor will fulfill common needs in research on cochlear implants and hearing aids at various laboratories around the world. It is our intent to make the present design widely available to interested and responsible investigators in the hope that significant duplication of effort and expenditure may be avoided.

2. Design criteria

Since the full range of candidate speech processing strategies cannot be anticipated, the design approach for achieving the broadest flexibility is to implement as much of the system as possible in software. Consequently, the hardware design should be as powerful and transparent as possible, given the presently available technology and the ergonomic limits on wearable equipment design. Options for future upgrades have been provided where possible.

The minimum design goals, listed roughly in order of priority, include:

(a) a system architecture consisting of a general purpose, transparent hardware front-end for conditioning analog audio signals and a powerful and flexible DSP engine for sampling of those signals and for implementation of speech processing algorithms in software;

(b) a processor able to control a variety of output drivers depending on the type of patient interface required;

(c) an inherently safe analog and digital design that provides for electrical safety, control of stimulation limits, and watchdog functions to monitor normal operation;

(d) small package size consistent with definition of a wearable unit;

(e) low power consumption so that battery size, weight and charging schedule do not interfere with daily use by patient;

(f) ease and simplicity of operation for the patient;

Specific to the immediate needs of the present project, the system provides:

(g) full software implementations of the continuous interleaved sampler (CIS) and the interleaved pulses (IP) speech processors;

(h) nonsimultaneous, pulsatile, current-controlled stimuli for delivery to 15 electrodes through a percutaneous connector;

(i) an interface for controlling the Nucleus transcutaneous transmission system.

3. DSP processor review and selection

Recently there has been a rapid increase in hardware available for implementation of DSP algorithms. There is broad choice among several vendors, as well as in the details of processor implementation (e.g. floating point versus integer). Although the present range of processing hardware is much wider than that of a few years ago, most current DSP machines have been designed for high processing speed at the cost of power consumption. In selecting a device suitable for a wearable system, however, power consumption is an important consideration. At the same time, we do not want to limit power consumption to the point that only marginal processor implementations can be achieved.

We have looked in detail at the available technologies and have concluded that the Motorola DSP56001 is the present device of choice. Primary advantages include its high speed and wide dynamic range (24 bits). It offers attractive power consumption features -- both in relatively low power demands and in options to minimize power consumption by altering the duty cycle of processor execution and by turning off portions of the processor architecture when not required. The device also is mature and from a well established company. Documentation is excellent and application support is good.

4. Functional block diagrams

This wearable speech processor system, intended to produce outputs with a variety of output driver configurations, has been designed for implementation on two circuit boards.

The first board features a general purpose, transparent front-end for conditioning analog audio signals and a powerful DSP engine for sampling and software implementation of the speech processing algorithm. Figure 1 is a functional block diagram of this signal processing board.

WEARABLE SPEECH PROCESSOR

Functional Block Diagram

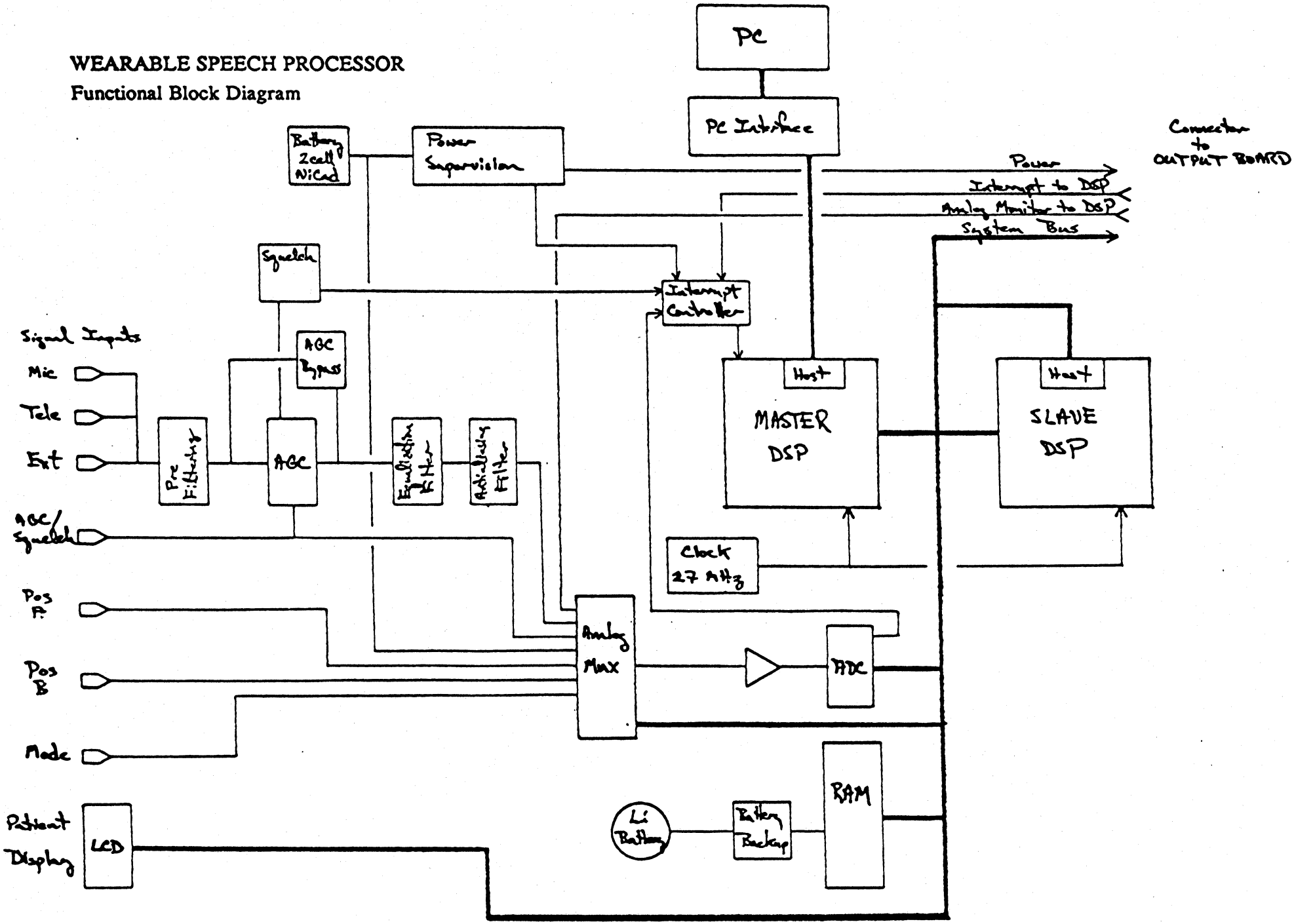


Fig. 1

A variety of output driver designs will exist for different research needs based on the method of patient stimulation. Each output driver will be configured on a second board that mates with the signal processor board. Figure 2 is a functional block diagram of a driver board for nonsimultaneous delivery of current-controlled pulses directly to 15 electrodes.

The designs for both the signal processing and output boards are implemented presently in breadboard form and are being tested and reviewed prior to construction of a set of printed circuit boards.

The processor system is programmed and controlled by a separate personal computer (PC) that interfaces with the signal processor.

The remainder of this report describes the elements of the block diagrams in additional detail. Front-end analog signal processing hardware is discussed first. Digital signal processor hardware design follows, along with a description of the multichannel output board design. A block diagram of a six-channel CIS processor is presented and benchmarks describing its implementation on this hardware platform are reported. A few notes on power consumption are included, and the basic elements of the controlling PC interface are described.

A future document will provide full schematics, results of system testing, processing benchmarks, and software coding examples.

B. Front-end processing hardware

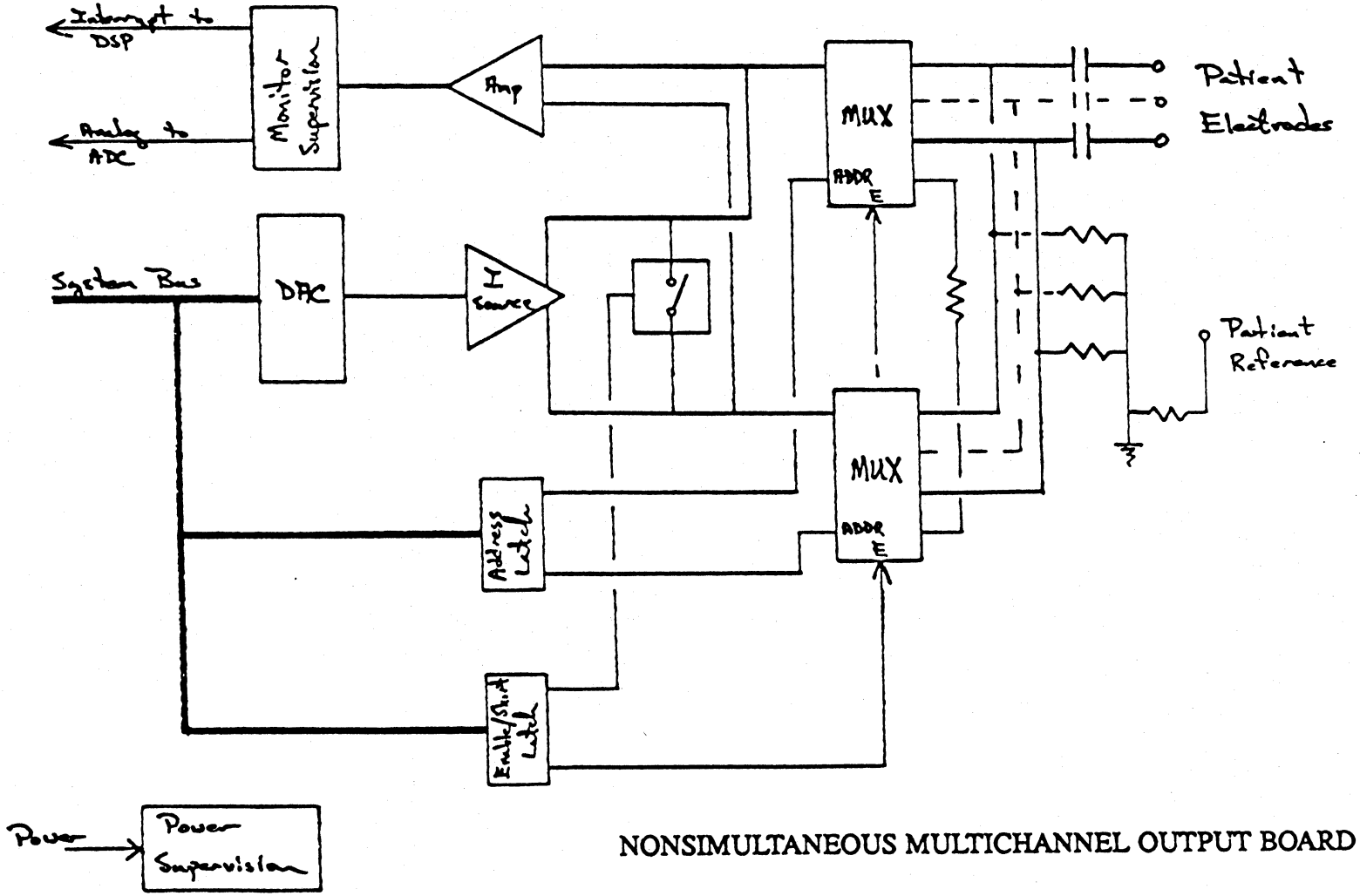
1. Signal input conditioning

Input signal options include a dedicated electret microphone, an inductive telephone pick-up, and a general purpose external input. Since output board options include direct electrical connection to implant patients with percutaneous connectors, provision must be made for safe electrical isolation for each of these input sources.

The present design will accommodate the addition of a dual channel input system to allow the use of two spatially separated microphones.

2. Automatic gain control (AGC)

Due to the wide range of signal levels in normal acoustic environments and the relatively narrow dynamic ranges of hearing of the hearing impaired, both acoustically and electrically, the use of a front end automatic gain control (AGC) is considered essential. A conventional slow AGC stage with fast attack and slow release times is appropriate. This type of compressor adequately equalizes input signal levels with minimal distortion of the temporal and spectral cues of speech.



NONSIMULTANEOUS MULTICHANNEL OUTPUT BOARD

Functional Block Diagram

Fig. 2

On the basis of availability, low power consumption, and functionality, the Gennum Corp. LD502 low distortion AGC compression amplifier has been selected. This component consists of a single-ended, inverting amplifier, with an internal current controlled feedback resistance for forward path gain setting. The AGC controlling current is derived by full wave rectification of the output signal. The attack time of the AGC circuit is fixed at less than 1 msec. The release time is adjustable from 40 to 500 msec by capacitor selection. The default release time in the present design is 500 msec.

Provision is made in hardware for defeating the operation of the AGC under software control. This feature would be used in the laboratory environment for patient and equipment testing with controlled inputs.

3. Spectral equalization

To minimize the loss of low amplitude, high frequency information in the speech signal due to sampling by limited magnitude resolution analog-to-digital converters, a speech equalization stage is included. This stage consists of a first order highpass filter, providing 6 dB/octave of equalization. The cutoff frequency and gain of this stage are resistor programmable.

The default corner frequency for the input filter is 10 kHz, providing full equalization across the speech band. Alternatives to full equalization can be achieved in the software of the DSP 56001. For instance, the equalization used in the IP and CIS processing strategies consists of a highpass filter that attenuates frequency components below 1200 Hz at 6 dB/octave. This characteristic can be realized on the DSP 56001 platform by processing the fully equalized input with a 1200 Hz lowpass filter implemented in software.

4. Antialiasing filter

The antialiasing filter consists of three cascaded filter stages, with components selected to provide a 6-pole, lowpass Butterworth characteristic with a cutoff frequency of 7.0 kHz. Forward path passband gain is 1.0. The measured output gain is -21.6 dB at 10kHz., -32.5 dB at 12 kHz., -45.0 dB at 14 kHz, and -52.0 dB at 16 kHz. The 6-pole Butterworth characteristic provides sufficient amplitude rolloff without excessive ringing.

5. Input multiplexer and analog-to-digital conversion

The input multiplexer is an eight channel, memory-mapped, address-latched CMOS device used for selecting among several input signal sources for A-to-D conversion. The input signal options include:

Channel	Signal
0	Equalized, antialiased speech (see section B.3 above)
1	Output Monitor (see section D on output board design)
2	Potentiometer A (see section B.7 on user interfaces)
3	Potentiometer B (see section B.7 on user interfaces)
4	Mode Switch (see section B.7 on user interfaces)
5	Battery Monitor (see section F.3 on power supervision)
6	Squelch Monitor (see section B.6 on squelch operation)
7	(not allocated)

Several ADC units are presently under consideration. A minimum sampling rate of 15 kHz (66.7 μsec between samples) is required for the antialiasing filter described in section B.4. ADC resolution of 12 bits is desired.

Two ADCs have been implemented on the breadboard. These are the 10-bit RCA CA3310 and the 13-bit TI ADC1225. Both units are being evaluated by examining the degree of spectral distortion introduced by each ADC. Continuous sinusoids are sampled and buffered in the DSP memory. Blocks of such data are passed to the PC and windowed. Then FFTs are computed to show the spectra of the sampled signals. Additional evaluations will be aimed at determining (a) the number of bits required to represent speech in realistic noisy environments and (b) the number of significant bits the front-end design can provide in terms of dynamic range and linearity.

Newly released 12-bit, low-power ADC's from Analog Devices and Burr Brown have been obtained and will be evaluated also.

6. Squelch operation

Squelching is functionally defined here as the cessation of output presentation when no stimulus of value to the patient is present. If these periods of effective silence can be predicted by front-end hardware processing, significant advantages can be gained in the operation of the equipment. Principal among these is the idling of the signal processor hardware during such periods to reduce battery drain. In this way, average power drain can be cut by 30 to 40 percent during typical conversation. Substantial additional savings can be gained during periods of prolonged silence. Another possible advantage of squelching is the discrimination between noise and signal-plus-noise conditions. This discrimination would allow the efficient implementation of spectral subtraction and other noise reduction algorithms in speech processor systems. The spectral subtraction algorithm is particularly effective in reducing interference due to quasi-stationary environmental noise.

The squelching operation implemented in this system is simple. Essentially all that is done is to amplify the voltage level across the AGC integrator capacitor and compare the

amplified signal with a reference voltage. If the amplified signal is greater than the reference, then a signal-plus-noise condition is signaled by the comparator.

The adjustment of the squelching threshold is effectively locked to the adjustment of the AGC threshold. The AGC threshold adjustment changes the input signal level at which the AGC starts reducing gain. Since the voltage level across the AGC integrating capacitor is the controlling signal for the AGC gain element, signal-plus-noise conditions correspond roughly to periods when the AGC is actively controlling the forward path gain.

7. Patient control interface

The operating controls available to the user should be as simple as possible. They should, however, be sufficiently numerous and flexible to support the research functions that the device is intended to provide. The presently proposed interface options include:

- Power ON/OFF - could be integrated into Mode Switch
- AGC/Squelch Control - potentiometer
- Potentiometer A - software readable level for arbitrary use
- Potentiometer B - software readable level for arbitrary use
- Mode Switch - 8 position switch that is software readable

A 2x16 character liquid crystal display (LCD) also is being considered for increased feedback to the patient.

C. Digital signal processor hardware design

1. Dual processor architecture

A dual processor design, using two DSP56001's, provides an extremely flexible and powerful architecture capable of implementing a wide range of processing strategies. This design exploits the integrated design features of the 56001 for multiprocessor operation.

a. Master/slave relationship

The two processors are configured in a master/slave relationship. The master processor computes the basic algorithm to implement the speech processor. A key activity for the master processor is to provide control signals for the output stimulus board. Normally the slave processor is stopped and consuming no power. On demand the slave may be activated (by an interrupt from the master) to perform computing tasks in parallel with the master. Once the slave has completed its task, it stops itself and waits for another interrupt.

The master and slave processors communicate via shared memory and by use of the host interface in the slave processor.

b. Interprocessor communications

i. Shared memory

The master and slave processors share memory by using the bus arbitration logic built into the 56001. When the slave processor makes an external memory access, the master receives a request to release the bus. The slave executes wait states until the master finishes its present bus cycle. At that point the master tristates its bus drivers and asserts the bus grant line. The bus grant line enables the tri-state buffers, allowing the slave processor to access the memory. The slave completes its memory access cycle and releases its original bus request, completing the process.

Communication by shared memory provides a fast and transparent method of inter-processor communication. This method will be used principally to transfer data but also may be used to transfer processing code to the slave processor's internal RAM for execution.

ii. Host interface options

The master processor may communicate with the slave using the latter's host interface. In this configuration the slave's host interface is memory mapped to the common memory space of both processors. The master, by making memory accesses, can control the slave's interface. The host interface can initiate three types of interrupts in the slave DSP. These are *host receive data*, *host transmit data* and *host command*. The first two interrupts alert the slave that the master has transferred data and in what direction. The host command interrupt can force the slave to execute any of thirteen subroutines. Primary among these routines would be subsections of a speech processor design, such as filtering, energy estimating, pitch extraction, etc. Some subroutines may be tasks to overwrite program code in the slave's internal RAM from code stored in the high RAM common to both master and slave, thus allowing the slave to be reprogrammed dynamically. At the completion of each subroutine initiated by the host, the slave would return to the stopped state and again consume minimal power.

2. Memory organization

This design uses RAM both internal and external to the 56001. Internal to each of the master and slave DSPs are 512 X 24 bits of on-chip program RAM. In addition, each processor has another 512 X 24 bits of on-chip data RAM apportioned equally between X and Y data spaces. On-chip peripherals are mapped into the high portion of the X data memory, and external peripherals are mapped into the high portion of the Y data memory. All on-chip RAM memory is zero wait state and volatile.

External to both the master and slave DSP are 32K X 24 bits of shared RAM. The memory is composed of three 32K X 8 bit CMOS RAMs (100 μsec access time) connected in parallel. These RAMs operate at three-wait-state speed and have battery backup, providing nonvolatile operation. The 32K X 24 bits of external RAM are segmented into 16K X 24 bits of program memory, 8K X 24 bits of X data memory, and 8K X 24 bits of Y data memory.

The 16K words of external program RAM map from locations $C000 to $FFFF. The 8K words of external X data memory map from $A000 to $BFFF. The 8K words of external Y data memory map from $8000 to $9FFF.

External peripherals are mapped to the high Y data memory from $FFC0 to $FFFF. This space is split into two portions. One is for external peripherals on the primary DSP board ($FFC0 to $FFC7) and the other is for external peripherals related to the family of output boards ($FFC8 to $FFFF). Address decoding logic is provided on the DSP board to indicate when an external peripheral is being accessed (HIY* asserted negative true). The specific peripheral address being accessed is determined by decoding address lines A0 - A5.

3. Interrupt architecture

External interrupts are managed by a hardware priority encoder. Eight interrupts of differing priority levels are allowed. All external interrupt signals are latched negative-true by their sources and are cleared only by reading or writing to the interrupt source by the DSP during interrupt servicing.

On receipt of an external interrupt, the priority encoder issues an interrupt to the IRQA interrupt line of the DSP. The priority level of the pending interrupt is available to be read by the DSP on lines 6, 7, and 8 of the C Port. The priority encoder is enabled by clearing line 1 of the C Port to zero. Setting line 2 of the C Port disables the squelch interrupt.

4. Reset/initialization operations

Reset/initialization options vary depending on whether the wearable processor is connected to the programming computer (PC) or not. In typical operation the processor will not be connected to the PC.

On power-up, initiated by turning the power switch on, a full system reset occurs. This reset forces the output board into a disconnected condition. The 56001 DSP is initialized in Mode 2, in which it begins operation at location $E000 of external program memory. An initialization/check-out software procedure begins executing at $E000 to prepare for and verify proper system operation.

When the wearable processor is not connected to the programming PC, system reset may be triggered by cycling the unit's power switch.

5. Host/PC interface

A separate, stand-alone PC is used to control and program the wearable processor. Since the wearable processor has static RAM with battery backup, programs downloaded from the PC are retained when DSP power is turned off. Hence the basic strategy is to connect the wearable processor to the PC, use the PC to develop the processing strategy, and download the strategy to the DSP for testing. Once the strategy is finalized, the unit is simply disconnected from the PC and the patient departs with the programmed wearable processor. This method of operation is greatly facilitated by using the host interface of the master 56001 (in the wearable device) to mediate communications with the PC. This interface is described in more detail in Section G, below.

6. Output board interface

As mentioned before, the output board interface is memory mapped on the master DSP bus. The output board is configured as an external peripheral operating with 24 bi-directional data lines and 6 address lines. Dedicated external interrupts to the master DSP also are provided from the external driver board. The following section more fully describes one output driver configuration.

D. Multichannel output hardware with single multiplexed current source

This output board features a single, digitally-controlled current source whose output is channeled through a multiplexer. The design features two basic sections. One is a forward path consisting of a digital-to-analog converter (DAC), a current source, and an output multiplexer for directing current to selected electrode pairs. The other is a return path consisting of amplifiers and peak voltage detectors for monitoring proper operation of the output board. Miscellaneous circuitry provides balanced power supplies and support logic.

Along the forward output path a 12-bit, latched, multiplying DAC converts two's complement digital code into a bipolar output signal. The DAC reference is fed by a 3.0 volt source. Amplitude and offset trimmers are provided for adjusting final forward path current calibration and minimizing the DAC's DC offset prior to the current source stage. The output of the DAC stage is capacitively coupled to the current source stage.

The current source consists of a single non-inverting amplifier stage. Current control is obtained by placing the patient's electrodes directly into the feedback loop of the amplifier. Current gain is determined by the *gain setting* resistor (R8), connected from the inverting input of the op-amp to ground. The current flowing in the feedback loop is equal to the voltage appearing at the non-inverting input divided by the resistor value. Gain typically is set so that 2.0 mA peak-to-peak currents are produced for maximum DAC outputs. High frequency gain of the feedback loop is rolled-off beginning at 50 kHz to stabilize the output circuit and guard against spurious oscillations occurring under open circuit load conditions. A resistive feedback

path in parallel with the patient load determines the DC gain.

The primary feedback path of the current source is routed through two 16-channel CMOS multiplexers to coupling capacitors which connect to the electrode leads. The channel assignments of each multiplexer may be set independently, allowing complete software control over the current source connection to the available patient electrodes. One channel on each multiplexer is assigned to a resistive dummy load for validating proper operation of the output board prior to activating the multiplexer output connections to the patient's electrodes. Consequently, a total of 15 electrodes may be used for patient stimulation.

E. CIS speech processor implementation

The CIS strategy has been described in detail in previous quarterly reports. A block diagram of the strategy is presented in Figure 3. A preprocessed signal is sampled by an ADC, as outlined in sections B.2 through B.5. All remaining processing then is implemented in software.

In software, the sampled speech signal is lowpass filtered at 1200 Hz (1st order) and then directed to a bank of six bandpass filters. Each bandpass filter has a sixth order Butterworth characteristic, with three poles per skirt. The output of each bandpass filter is rectified, either full- or half-wave, and then lowpass filtered by a first order smoothing filter.

The outputs of the smoothing filters provide a set of reference signals for generating a sequential series of biphasic pulses on each output channel to the patient's electrodes. The pulses are amplitude modulated based on the instantaneous signal level of each channel's smoothing filter output. Figure 4 shows the basic temporal sequence of thirteen events necessary to construct an output pulse on each of six channels. Each event is triggered by an internal interrupt from the onboard interval timer of the master DSP. Typically interrupts occur every 50 to 100 microseconds. Beginning with event 1 and progressing in sequence as interrupts occur, the following actions are taken:

Event 1 -

- Zero DAC for previous channel.
- Send data to the MUX address latch to direct the multiplexers to the electrode pair for channel 1.
- Use smoothing filter output for first channel as an index for a table lookup to implement instantaneous mapping law.
- Send new pulse height to output board DAC beginning to drive current across the selected electrodes in the initial phase of a biphasic pulse.
- Store negative of pulse height for the second phase magnitude for subsequent output.

DSP 56001 SPEECH PROCESSOR DIAGRAM

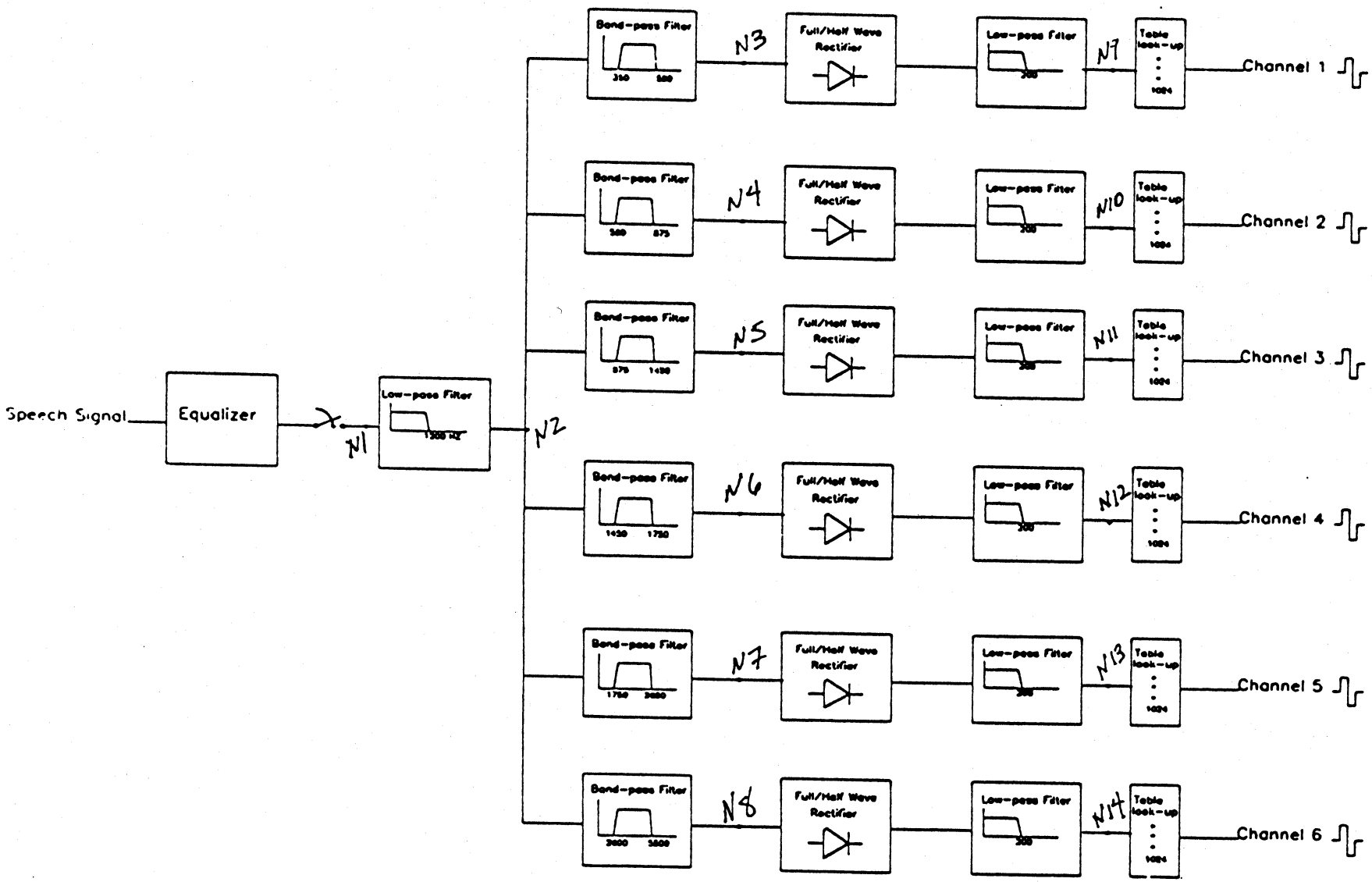


Fig. 3

PULSE GENERATION

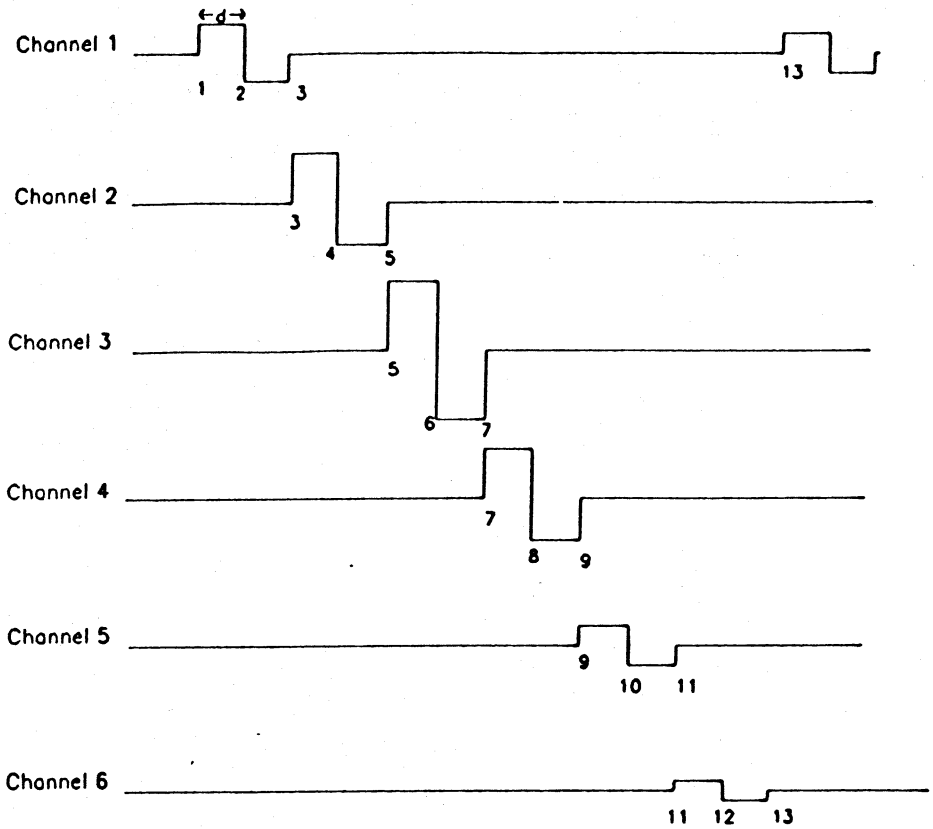


Fig. 4

Event 2 -

- Send saved pulse height to DAC to begin the second phase of the channel 1 pulse.

Event 3 -

- Zero DAC for channel 1, terminating the biphasic pulse.
- Wait 2 microseconds to let current source slew to zero.
- Send data to the MUX address latch to direct the multiplexers to the electrode pair for channel 2.
- Use smoothing filter output for second channel as an index for a table lookup to implement instantaneous mapping law.
- Send new pulse height to output board DAC beginning to drive current across electrodes for channel 2.
- Store negative of pulse height for the second phase magnitude for subsequent output to channel 2.

Event 4 -

- Send saved pulse height to DAC to begin the second phase of the channel 2 pulse.

Event 5 -

- Zero DAC . . . . . .

.
.
.
.

Repeat steps looping back to channel 1 after finishing with channel 6.

As a rough benchmark, we note that approximately 40% of the computing resources of the master DSP 56001 are required to implement the 6-channel CIS processor just described. A complete filtering cycle is initiated every 67 microseconds (i.e., at the 15 kHz sampling rate of the ADC). The full program executes in 398 words of on-board RAM. Lookup tables for implementation of precomputed mapping laws require 6143 words of external data memory with another 200 words of internal data memory used for storage of variables and filter coefficients. A slave DSP 56001 is not required for this particular strategy.

F. Power supply design

Since this equipment will be battery operated, considerations relating to electrical power consumption are especially important in the overall design. Fortunately, along with the recent advances in DSP technology, there have been significant developments in battery technology and DC power conversion devices. The following sections summarize estimates of required power, battery options and expected run times between battery replacements. Finally, a brief review is given of the power conversion circuitry in the present design.

1. Power budget

All power consumption estimates presented here are based on direct measurements from the prototype breadboard. Further reductions in power consumption are expected as portions of the design are optimized and the intrinsic power reduction features of the DSP (sleep modes and adjustable wait states) are implemented in the speech processor code.

Front end with ADC		40 mW
Single 56001 @ 27 MHz executing a 6-channel CIS strategy		
running continuously		500 mW
running continually with squelching		250 mW
Output board (single current source with nonsimultaneous multiplexed output)		200 mW
Totals	continuous	740 mW
	with squelching	490 mW

2. Battery selection and operation times

A wide variety of battery options are available. The design allows the use of either disposable or rechargeable batteries. The disposable battery of choice is the alkaline cell due to its high energy density and availability. However, operating times will be limited due to the relatively large power requirements of the speech processor system. The accumulating costs of alkaline battery purchases could prove unacceptable, especially if the user of the device is bearing the expense. As a lower cost alternative, rechargeable Nickel-Cadmium (NiCad) cells may also be used, but with the inconvenience of more frequent battery changes and the probable need to carry a supply of recharged batteries. In any case, the final battery choice will depend upon a variety of factors, including the system power demands (largely dictated by the complexity and computational needs of the processing strategy), convenience to the device

user, and battery replacement costs.

The following tables summarize the expected performance from readily available "D" size cells, both alkaline and NiCad.

Single "D" NiCad (High Capacity Type "E")	1.2 V x 4.4 AHr	= 5.3 W-Hr
$14.00 each (100 recharges)		
Two "D" NiCads		= 10.6 W-Hr
Single "D" Alkaline (Standard)	1.5 V x 0.32 A x 31 Hr	= 14.9 W-Hr
$1.10 in small volumes		
Two "D" Alkalines		= 19.8 W-Hr

Assuming an 80% conversion efficiency for the DC-to-DC step-up converter:

one cell (NiCad) ..... 5.3 W-Hr --> 4.2 W-Hr
two cells (NiCad) .....10.6 W-Hr --> 8.4 W-Hr

one cell (Alkaline)....14.9 W-Hr --> 11.9 W-Hr
two cells (Alkaline)...29.8 W-Hr --> 23.8 W-Hr

Operation time estimates

Single 56001 @ 27 MHz executing a 6-channel CIS strategy

a. Continuous operation (740 mW):

one cell (NiCad) ..... 4.2 W-Hr --> 5.7 Hr
two cells (NiCad) ..... 8.4 W-Hr --> 11.4 Hr

one cell (Alkaline)....11.9 W-Hr --> 16.1 Hr
two cells (Alkaline)...23.8 W-Hr --> 32.2 Hr

b. Operation with squelching (490 mW):

one cell (NiCad) ..... 4.2 W-Hr --> 8.6 Hr
two cells (NiCad) ..... 8.4 W-Hr --> 17.2 Hr

one cell (Alkaline)....11.9 W-Hr --> 24.3 Hr
two cells (Alkaline)...23.8 W-Hr --> 48.6 Hr

3. Power conversion and supervision

Power is generated by converting upward from a low-voltage battery stack to produce +5 volts for the DSP chip and support electronics. The Maxim MAX658 converter is being used to convert from a two battery stack to produce 750 mW at 5 volts with 75-80% efficiency. Use of a three battery stack to obtain higher transfer efficiency is being evaluated also. In circuit areas where greater operating voltages are required (e.g., the output board current driver requires +/- 10 volts) dedicated DC-to-DC charge pumps are used as needed to convert from the +5 system rail.

Dedicated hardware battery monitors are used to initiate safe shut-down procedures at the end of battery life. The static RAM battery backup is provided by a dedicated 3-volt lithium cell, which automatically is switched in when the +5 system rail drops below the lithium cell voltage.

G. Host/PC Interface

The purpose of the Host/PC Interface is to provide a mechanism for reading and writing to the DSP memory, reading monitoring status signals regarding power and cabling, and controlling the reset/mode signals of the DSP.

1. Hardware considerations

The Host/PC Interface consists of two boards: the *Host Interface PC Board*, which resides in the Host Computer (the PC), and the *Host Interface Isolation Board*, which is located in a separate box outside the PC. The Host Interface PC Board buffers and decodes control signals from the PC bus and provides the decoded control signals, buffered address lines, and buffered data lines for data transfer to the Host Interface Isolation Board. The Host Interface Isolation Board optically isolates these signals so that data may be passed safely between the Host PC and the DSP board. The Host Interface Isolation Board additionally monitors the status of the DSP Board and provides decoding and driving circuitry for controlling the mode pins of the DSP56001.

2. Software considerations

An extensive MONITOR program has been written for execution on the PC to control the DSP system in the laboratory. This MONITOR program also has been used during breadboard design development, allowing discrete control of hardware features from high level 'C' code running on the PC.

The detailed operation of the MONITOR is beyond the scope of this brief report. To convey a sense of the features included in the MONITOR program, however, four menus of available options are presented below.

MONITOR Software Menus:

- Main Menu -

Commands:	*gp addr*	*get program memory at hex address addr*
	pp addr data	*put program data to hex address addr*
	gx addr	*get X memory at hex address addr*
	px addr data	*put X data to hex address addr*
	gy addr	*get Y memory at hex address addr*
	py addr data	*put Y data to hex address addr*
	goto addr	*goto hex address addr*
	swreset	*DSP software reset*
	m2reset	*mode 2 hardware reset*
	waitenter	*wait mode*
	stopenter	*stop mode*
	icr	*read interrupt control register (ICR)*
	isr	*read interrupt status register (ISR)*
	readrx	*read DSP RX registers*
	writetx	*write to DSP TX registers*
	repeat	*repeat last instruction until a key is hit*
	test	*display test menu*
	ad	*display A/D menu*
	outboard	*display output board menu*
	maplaw	*load mapping law*
	memload	*load DSP memory from a file*
	restart	*restart this program*
	bootstrp	*send bootstrap file to DSP and restart*
	quit	*quit from this Monitor program*
	?	*display monitor commands (this menu)*

- Test Menu -

Commands:	*tpd addr*	*test program data path via location addr in program memory*
	txd addr	*test x data path via location addr in x memory*
	tyd addr	*test y data path via location addr in y memory*
	waits reg	*set reg (hex) value for wait states control* *4 nibbles --> (extX extY extP extI/O) each (0-f)*
	quit	*return to main menu*
	?	*display monitor test commands (this menu)*

- AD Menu -

Commands:	*cal*	*Send self-calibration command to A/D Converter*
	sample	*Send convert command to A/D Converter and display value*
	block rate	*Collect a block of A/D data and write it to a file*
	quit	*return to main menu*
	?	*display monitor A/D commands (this menu)*

- Output Board Menu -

Commands:	*discon*	*activate disconnect line*
	open	*open shorting switch*
	close	*close shorting switch*
	enabmux	*enable output MUX*
	dismux	*disable output MUX*
	mux addr	*set output MUX address to addr (00-FF)*
	dac value	*set DAC to value (000-FFF)*
	mon addr	*set monitor MUX address to addr (0-7)*
	trig	*trigger an interrupt flag*
	status	*read status and display (in hex)*
	dur value	*set pulse duration of value (decimal) μsec per phase*
	pulse	*output one biphasic pulse (pos leading)*
	pulses	*output one biphasic pulse (pos leading) and set shorting switch at end*
	sweepb	*sweep current pulse structure across electrodes in bipolar fashion according to data in sweepb.dat*
	sweepm	*sweep current pulse structure across electrodes in monopolar fashion according to data in sweepm.dat*
	quit	*return to main menu*
	?	*display monitor output board commands (this menu)*

III. Plans for the Next Quarter

Our plans for the next quarter include the following:

1. Presentation of project results in two papers at the *1991 Midwinter Meeting of the Association for Research in Otolaryngology*, to be held in St. Petersburg, FL, February 3-7.
2. Completion of the isolated interface and shell program for the DSP 56001 system (see Introduction points 4 and 5).
3. Completion of automated testing procedures for functional evaluations of CIS processor implementations.
4. Full evaluation of the prototype portable processor with patient SR2, to confirm that speech performance using the portable processor is comparable to that obtained in past studies using a laboratory system based on the TMS320 device (see *QPRs* 2 and 4, this project).
5. Continued studies with patient UP3, for further evaluation of CIS processors and for measurement of electric fields produced in the scala tympani with various electrodes and electrode combinations (measures of field potentials will be made via unstimulated electrodes).
6. Continued collaboration with investigators at the House Ear Institute, on further studies with auditory brainstem implant (ABI) patients.
7. Continued preparation of manuscripts for publication.

IV. Personnel

We are pleased to introduce a new member of our technical staff for this project, Mariangeli Zerbi, who joined the team on November 26. She earned her Bachelor's degree in electrical engineering from Georgia Institute of Technology with highest honors, and her Master's degree in the same field from Stanford University. After completing her Master's degree, she worked for several years at ETEC Corporation in Hayward, California. Her primary responsibilities there were software and hardware development for systems using the 68020 microprocessor and for systems using multiple DSP 56001 processors. The latter experience is directly relevant to our own use of the DSP 56001, as described in this report. Finally, Ms. Zerbi has a background of coursework in physiology and biomedical engineering. She already has written much of the software for the prototype portable processor, and we expect that she will make many other important contributions to our efforts in the coming years.

In addition to Ms. Zerbi, Dr. Chris van den Honert and Mr. Dean Hering helped us with the work described in this report. Dr. van den Honert is a new consultant to our overall project, and has many years of experience in the development of speech processors for auditory prostheses. He provided guidance on the design of the power supervision circuitry for the present prototype processor. Mr. Hering is with the Center for Technology Applications at RTI, and has a Master's degree in electrical engineering from Carnegie Mellon University. His industrial experience includes design of hardware and software for complex monitoring systems using multiple 68020 processors. His primary responsibility for the present work was to design the interfaces and software for communication between a controlling PC and the master DSP 56001 in the wearable unit. He also designed the isolation circuits for safe operation of the integrated system (with the controlling PC connected) during patient testing.

The entire effort was supervised by Dr. Finley.

Appendix 1

Summary of Reporting Activity for the Period of

November 1, 1990 through January 31, 1991

NIH Contract N01-DC-9-2401

Reporting activity for the last quarter included an invited lecture and a short publication, listed below. The publication is reproduced on the next two pages.

Javel, E. and C.C. Finley (1990) Review of Program Project Grant, "Mechanisms of Intracochlear Electrical Stimulation." *Surgical Grand Rounds*, Duke University Medical Center, November. [This presentation also reviewed recent findings from the Speech Processors project, N01-DC-9-2401.]

Finley, C.C. (1990) Radial bipolar electrode placement in scala tympani: Effects on neural potential profiles and longitudinal spread of excitation. In *Proc. Twelfth Ann. Conf. Engineering in Medicine and Biology Soc.*, IEEE Press, New York, pp. 2290-2291.

RADIAL BIPOLAR ELECTRODE PLACEMENT IN SCALA TYMPANI:
Effects on neural potential profiles and longitudinal spread of excitation

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ABSTRACT

A three-dimensional, finite-element field model of intracochlear electrical stimulation using a pure radial, bipolar electrode configuration is presented. Fiber potential profiles and longitudinal potential spread functions to a step function electrode potential input are evaluated with regard to placement of the electrode array within scala tympani.

These model results suggest that bipolar electrode placement within scala tympani significantly affects the potential patterns created in the vicinity of the neural elements. In the particular case where the bipolar electrode is near the lateral wall of scala tympani, uniform, nearly constant potential profiles are generated near the fibers and many of the unique defining characteristics of the bipolar electrode configuration are effectively lost.

INTRODUCTION

Previous work using three-dimensional finite-element models of intracochlear field patterns generated by pure radial bipolar electrode arrays have assumed that the array was placed on the modiolar wall of scala tympani near the target neural fibers [1,2]. This placement is considered ideal for minimizing the spread of current to tissue regions near adjacent electrode pairs in multichannel cochlear prostheses, thus reducing the confounding effects of channel interactions. Placement of the electrodes in this position may or may not be achieved in actual surgery due to anatomical variations and/or bone growth. The effects of variable placement of the electrode array within scala tympani on electrical field patterns near target neurons are examined here.

METHODS

In this finite-element model a cross section of the cochlea is projected linearly along an axis perpendicular to the plane of the section, thus producing a short, straight segment of the cochlea. A radially-oriented bipolar electrode pair, mounted in a carrier insulator is located in scala tympani. See [1] and [2] for complete details for this model. Element resistivities (in ohm-cm) are defined regionally to characterize the electrodes (0.1), the carrier insulator (10^9), the endolymph (60), the perilymph (70), Reisner's membrane (60480), basilar membrane (1800), the anisotropic neural tissue of the peripheral axon leading down from the habenula to the spiral ganglion (300 axial; 1500 transaxial), the spiral ganglion (300) and bone (630). Fixed potentials (+/- 100 mV)are assigned to the electrode surfaces and the resulting field patterns computed [1,2].

The results for medial, lateral and baso-lateral positioning of the electrode array are shown in the three columns of Fig 1. Panel (a) shows the assumed placement of the electrode array within scala tympani. Panel (b) shows the potential profiles along selected fibers at various longitudinal positions along the cochlea. Relative fiber locations are indicated at the top of panel (c). Panel (c) shows the spread of potentials along the longitudinal axis at fixed fiber node positions. Relative node positions are indicated in panel (a) and at the top of panel (b).

DISCUSSION

In the medial position, the pure radial configuration creates a distinct pattern of potential gradients along the length of the distal axonal segment. As the electrode is moved laterally, the pattern shifts to a predominately isopotential pattern except at the very tip of the fiber where a steep gradient exists. When the electrode is moved basally, the steep gradient at the tip is lost.

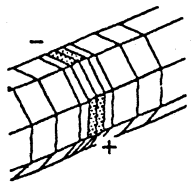
A sharp spread function is seen in both the medial and lateral positions, at least for the cathodic electrode. In the baso-lateral position the potential spread is much broader.

CONCLUSIONS

The electrical field patterns generated in the vicinity of the distal axonal processes by scala tympani bipolar electrodes are very dependent upon placement of the bipolar electrodes within scala tympani. Changes in placement of the electrodes produces significant changes in the level and distribution of extracellular potentials along the course of neural fibers and in the rate of field decay longitudinally along the cochlear partition. In the lateral and baso-lateral positions, the electrodes produce uniform, near constant potential profiles that differ significantly from the high magnitude, steep gradient profiles generated with the electrodes in the medial position. In addition, as the electrode is positioned further from the neural fibers, the rate of longitudinal field decay is reduced.

REFERENCES

1. Finley C (1989): A finite-element model of radial bipolar field patterns in the electrically stimulated cochlea - two and three dimensional approximations and tissue parameter sensitivities. IEEE/11th Conf. EMBS, 1059-1060.
2. Finley C, Wilson B and White M (1989): Models of neural responsiveness to electrical stimulation.



PURE RADIAL CONFIGURATION

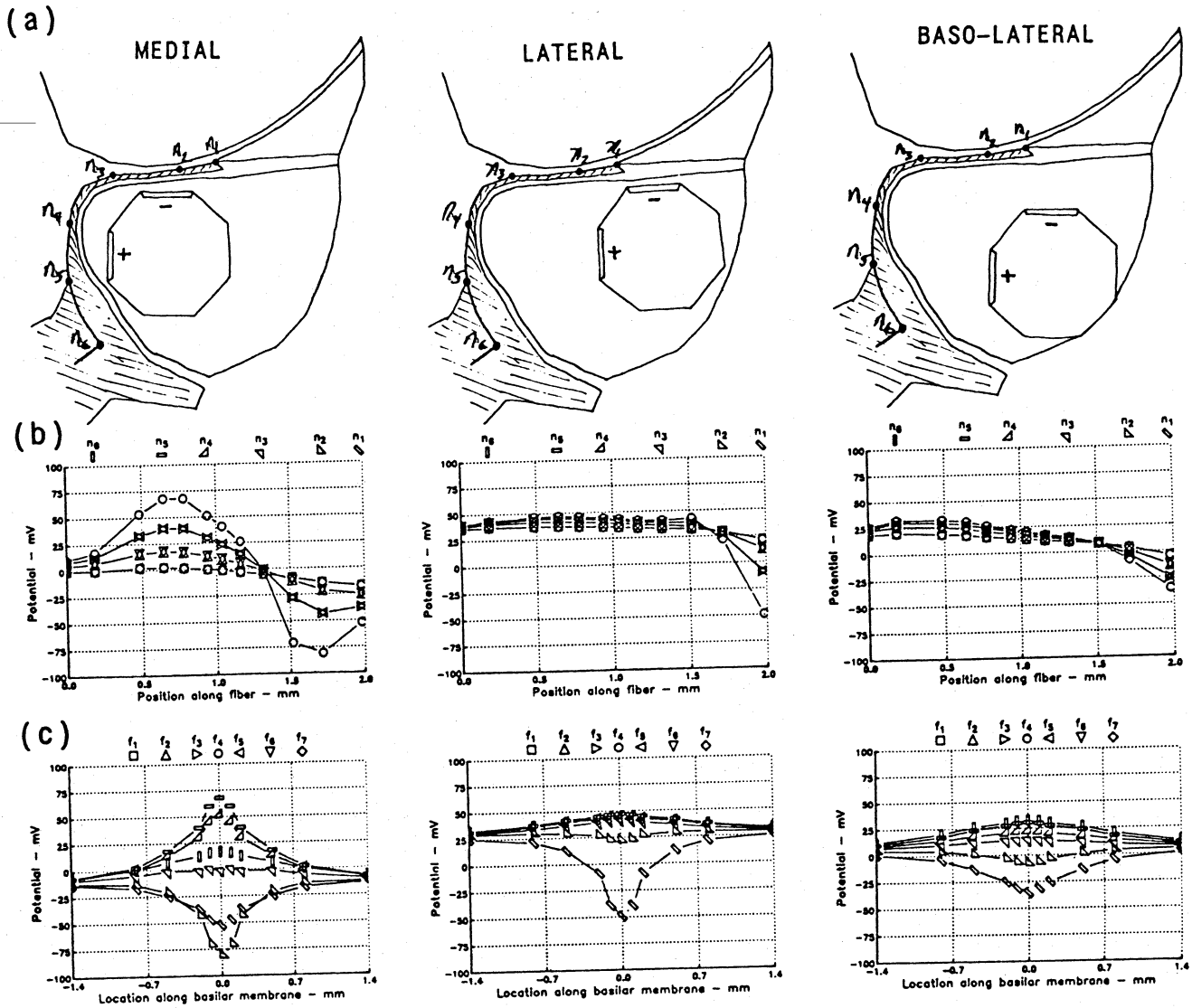


Figure 1. Scala tympani electrode placement and computed field potentials. Panel (a) indicates the relative position of an 800 micron diameter electrode carrier within scala tympani for each condition. Locations of nodes (n_1-n_6) along peripheral axon are indicated. Panel (b) shows computed extracellular potentials plotted as a function of position along the fiber for seven fibers spaced longitudinally along basilar membrane. Panel (c) shows computed extracellular potentials plotted as a function of longitudinal location for each node position (n_1-n_6).

Chapter 5 in Cochlear Implants - Models of the Electrically Stimulated Ear, (Miller JM and Spelman FA, eds), Springer-Verlag, pp. 55-96.

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